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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,132	03/16/2004	Conrado Blasco Allue	550-535	9239

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EXAMINER	
IQBAL, NADEEM	
ART UNIT	**PAPER NUMBER**
2114	

DATE MAILED: 09/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/801,132	ALLUE ET AL.	
	Examiner	Art Unit	
	Nadeem Iqbal	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 15, 16, & 29 are rejected under 35 U.S.C. 102(e) as being anticipated by Dervisoglu et al., (U.S. Patent number 6964001).

1. As per claim 1, Dervisoglu teaches (col. 2, lines 60-63) an integrated circuit logic blocks, a control unit, a memory associated with the control unit, the memory holds instructions for the control unit to perform test and debug operations of the logic blocks. He thus teaches an integrated circuit comprising a data processing circuit, a processor operable to perform processing under program instruction control, a diagnostic circuit coupled to the data processing circuit. With reference to diagnostic circuit operable to capture diagnostic data. He teaches (col. 2, lines 65-67). With reference to processor operable to access the diagnostic data relating to the data processing circuit. He teaches (col. 3, lines 5-7, col. 5, lines 1-3).

2. As per claim 2, With reference to the diagnostic circuit is operable upon detecting predetermined conditions to halt data processing by the data processing circuit. He teaches (col. 6, lines 29-31).

3. As per claims 15 & 29, Dervisoglu substantially teaches the claimed invention as disclosed related to claim 1 above. He also teaches (col. 2, lines 60-63) an integrated circuit logic blocks, a control unit, a memory associated with the control unit, the memory holds instructions for the control unit to perform test and debug operations of the logic blocks. He thus teaches an integrated circuit comprising a data processing circuit, a processor operable to perform processing under program instruction control, a diagnostic circuit coupled to the data processing circuit. With reference to diagnostic circuit operable to capture diagnostic data. He teaches (col. 2, lines 65-67). With reference to processor operable to access the diagnostic data relating to the data processing circuit. He teaches (col. 3, lines 5-7, col. 5, lines 1-3).

4. As per claim 16, With reference to the diagnostic circuit is operable upon detecting predetermined conditions to halt data processing by the data processing circuit. He teaches (col. 6, lines 29-31).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 3-14, 17-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dervisoglu et al., (U.S. Patent number 6964001) in view of Chen et al., (U.S. Patent number 5642478).

8. As per claim 3, Dervisoglu does not explicitly discloses that the diagnostic circuit operable to capture diagnostic code profiling data relating to program instructions. Chen teaches (col. 5, lines 43-45) a multimode system a dedicated capture circuit for capturing event data under software control within each node. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to include the invention of Chen into the invention of Dervisoglu to capture diagnostic code profiling data relating to program instructions. This is because both inventions are in the same environment of diagnosing and debugging. Dervisoglu also teaches (col. 5, lines 26-28) logic probe that captures sequences of digital signals from internal points of the IC.

9. As per claim 4, With reference to detecting predetermined conditions to trigger the data processing circuit to execute an exception handling program. Dervisoglu teaches (col. 6, lines 49-53).

10. As per claims 5 & 6, With reference to the processor is operable to control output of the diagnostic data relating to the data processing circuit from the integrated circuit. Dervisoglu teaches (col. 5, lines 1-5).

11. As per claims 7 & 8, With reference to the data processing circuit and the processor communicate during non-diagnostic operation via a system bus. Dervisoglu teaches (col. 12, lines 10-12).

12. As per claim 9, With reference to communicating during diagnostic operation via the system bus, the bus bridge and diagnostic bus. Dervisoglu teaches (col. 6, lines 12-16).

13. As per claim 10, With reference to storing the diagnostic data relating to the data processing circuit within memory mapped storage. Chen teaches (col. 7, lines 39-42).

14. As per claim 11, With reference to detecting predetermined conditions to halt program instruction execution by the processor and capture diagnostic data. Dervisoglu teaches (col. 6, lines 47-49).

15. As per claims 12 & 13, With reference to the providing data communication with an external operational device coupled to the integrated circuit. Dervisoglu teaches (col. 6, lines 24-26).

16. As per claim 14, Dervisoglu teaches (col. 2, lines 60-63) an integrated circuit logic blocks, a control unit, a memory associated with the control unit, the memory holds instructions for the control unit to perform test and debug operations of the logic blocks.

17. As per claim 17, Dervisoglu does not explicitly discloses that the diagnostic circuit operable to capture diagnostic code profiling data relating to program instructions. Chen teaches (col. 5, lines 43-45) a multimode system a dedicated capture circuit for capturing event data under software control within each node. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to include the invention of chen into the invention of Dervisoglu to capture diagnostic code profiling data relating to program

instructions. This is because both inventions are in the same environment of diagnosing and debugging. Dervisoglu also teaches (col. 5, lines 26-28) logic probe that captures sequences of digital signals from internal points of the IC.

18. As per claim 18, With reference to detecting predetermined conditions to trigger the data processing circuit to execute an exception handling program. Dervisoglu teaches (col. 6, lines 49-53).

19. As per claims 19 & 20, With reference to the processor is operable to control output of the diagnostic data relating to the data processing circuit from the integrated circuit. Dervisoglu teaches (col. 5, lines 1-5).

20. As per claims 21 & 22, With reference to the data processing circuit and the processor communicate during non-diagnostic operation via a system bus. Dervisoglu teaches (col. 12, lines 10-12).

21. As per claim 23, With reference to communicating during diagnostic operation via the system bus, the bus bridge and diagnostic bus. Dervisoglu teaches (col. 6, lines 12-16).

22. As per claim 24, With reference to storing the diagnostic data relating to the data processing circuit within memory mapped storage. Chen teaches (col. 7, lines 39-42).

23. As per claim 25, With reference to detecting predetermined conditions to halt program instruction execution by the processor and capture diagnostic data. Dervisoglu teaches (col. 6, lines 47-49).

24. As per claims 26 & 27, With reference to the providing data communication with an external operational device coupled to the integrated circuit. Dervisoglu teaches (col. 6, lines 24-26).

25. As per claim 28, Dervisoglu teaches (col. 2, lines 60-63) an integrated circuit logic blocks, a control unit, a memory associated with the control unit, the memory holds instructions for the control unit to perform test and debug operations of the logic blocks.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nadeem Iqbal whose telephone number is (571)-272-3659. The examiner can normally be reached on M-F (8:00-5:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571)-272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nadeem Iqbal
Primary Examiner
Art Unit 2114

NI